FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C906 • MM74C907 Hex Open Drain N-Channel Buffers • Hex Open Drain P-Channel Buffers

General Description

The MM74C906 and MM74C907 buffers employ monolithic CMOS technology in achieving open drain outputs. The MM74C906 consists of six inverters driving six N-channel devices; and the MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors.

All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- High current sourcing and sinking open drain outputs

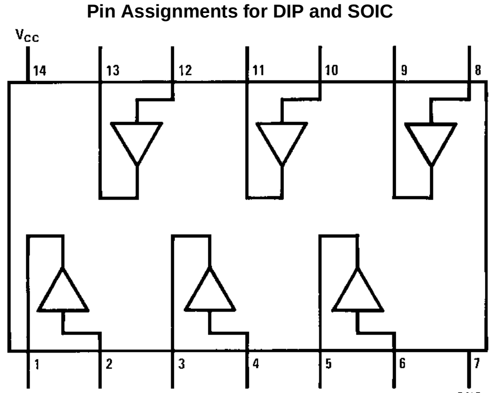
Ordering Code:

Order Number	Package Number	Package Description
MM74C906M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
MM74C906N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM74C907N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram

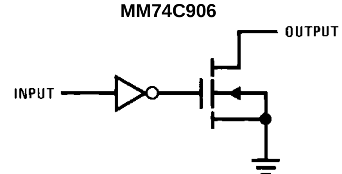
Pin Assignments for DIP and SOIC



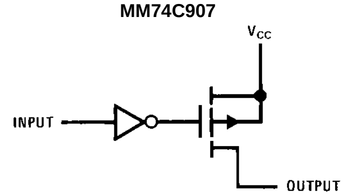
Top View

Logic Diagrams

MM74C906



MM74C907



Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	–0.3V to V_{CC} +0.3V
Voltage at Any Output Pin	
Operating Temperature Range	
MM74C906/MM74C907	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V, Output Open		0.05	15	µA
	Output Leakage					
	MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC} – 1.5V		0.005	5	µA
		V_{CC} = 4.75V, V_{OUT} = 18V				
	MM74C907	V_{CC} = 4.75V, V_{IN} = 1V + 0.1 V_{CC}		0.005	5	µA
		V_{CC} = 4.75V, V_{OUT} = V_{CC} –18V				
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} – 1.5V			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE CURRENT						
	MM74C906	V_{CC} = 4.75V, V_{IN} = 1V +0.1 V_{CC}				
		V_{CC} = 4.75V, V_{OUT} = 0.5V	2.1	8.0		mA
		V_{CC} = 4.75V, V_{OUT} = 1.0V	4.2	12.0		mA
	MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC} –1.5V				
		V_{CC} = 4.75V, V_{OUT} = V_{CC} – 0.5V	–1.05	–1.5		mA
		V_{CC} = 4.75V, V_{OUT} = V_{CC} – 1V	–2.1	–3.0		mA
	MM74C906	V_{CC} = 10V, V_{IN} = 2V				
		V_{CC} = 10V, V_{OUT} = 0.5V	4.2	–20		mA
		V_{CC} = 10V, V_{OUT} = 1V	8.4	–30		mA
	MM74C907	V_{CC} = 10V, V_{IN} = 8V				
		V_{CC} = 10V, V_{OUT} = 9.5V	–2.1	–4.0		mA
		V_{CC} = 10V, V_{OUT} = 9V	–4.2	–8.0		mA

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM74C906	V_{CC} = 5.0V, R = 10k			150	ns
		V_{CC} =10V, R = 10k			75	ns
	MM74C907	V_{CC} = 5.0V (Note 3)			150 + 0.7 RC	ns
		V_{CC} = 10V (Note 3)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM74C906	V_{CC} = 5.0V (Note 3)			150 + 0.7 RC	ns
		V_{CC} = 10V (Note 3)			75 + 0.7 RC	ns
	MM74C907	V_{CC} = 5.0V, R = 10k			150	ns
		V_{CC} = 10V, R = 10k			75	ns
C_{IN}	Input Capacitance	(Note 4)		5.0		pF
C_{OUT}	Output Capacity	(Note 4)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 5) Per Buffer		30		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.

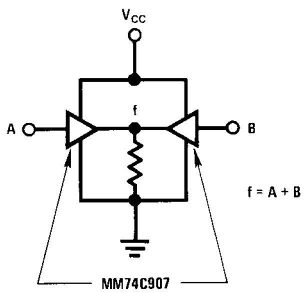
Note 3: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note, AN-90. (Assumes outputs are open).

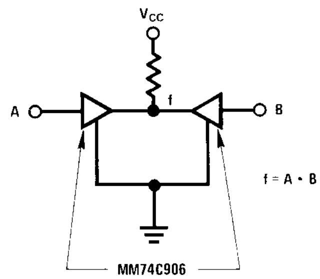
Typical Applications

Wire OR Gate



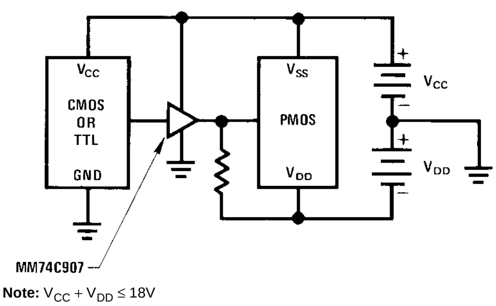
Note: Can be extended to more than 2 inputs.

Wire AND Gate



Note: Can be extended to more than 2 inputs.

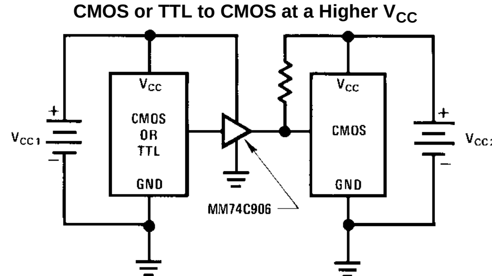
CMOS or TTL to PMOS Interface



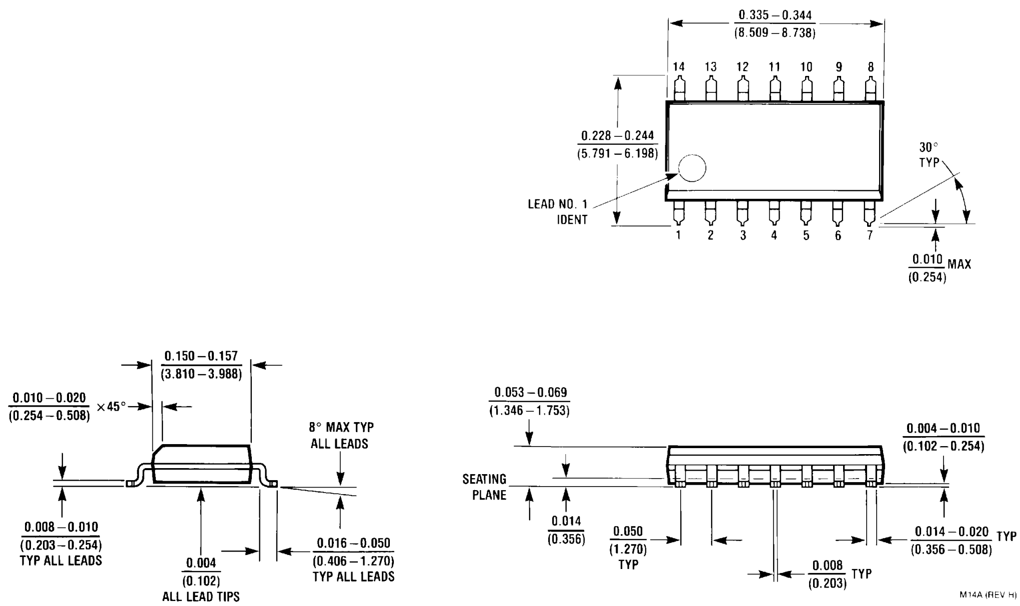
Note: $V_{CC} + V_{DD} \leq 18V$

$V_{CC} \leq 15V$

CMOS or TTL to CMOS at a Higher V_{CC}

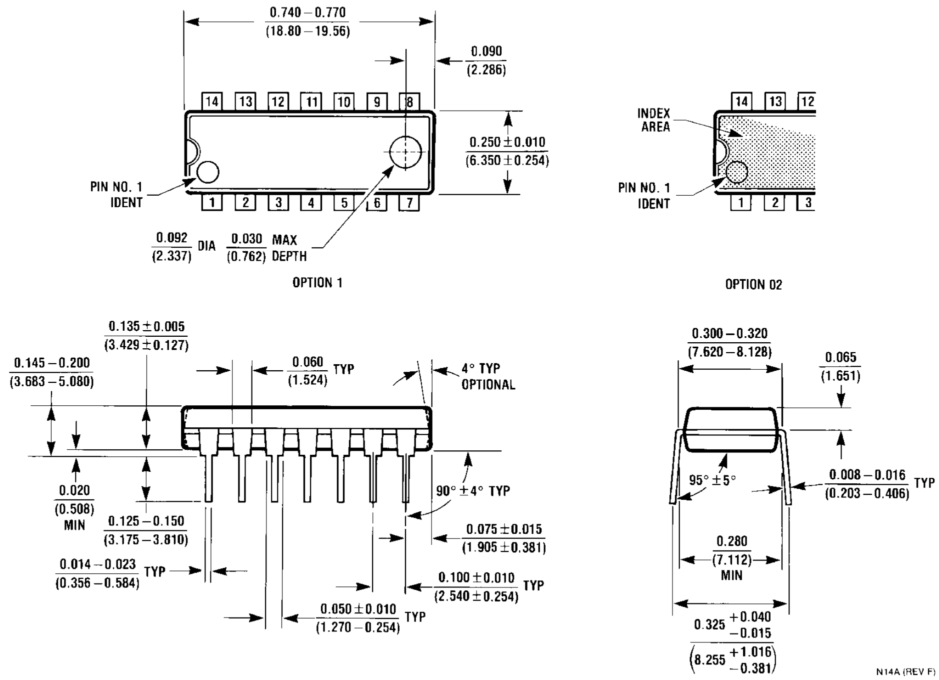


Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N14A

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